# 1. Executive Summary

TTP Meteor Ltd is part of the Technology Partnership Group, a technology development and innovation centre, located in the Melbourne Science Park near Cambridge. The Technology Partnership was created 25 years ago and now the enterprise has grown and evolved into TTP Group, where a range of technical and businesses take place. TTP Group provides a broad range of product and service in various market sectors, covering medical devices, aerospace and defence, communications, digital printing, etc. New companies are created inside the group and TTP Meteor Ltd is one of them.

TTP Meteor is specialised in providing powerful and flexible driver solutions for industrial printheads. Today’s industrial-used printheads are demanding and sophisticated devices, with high requirements on precision, quality, print speed and scale, which affects the quality and efficiency of manufacturing process. Different printheads electronics and software must be optimised to achieve best performance. TTP Meteor provides a flexible but powerful architecture, associating various printheads to Meteor PrintEngine Software, which can be re-configured simply to meet the changing and evolving environment in printing market, including ceramics, textiles, wide format, labelling and digital press.

My project in TTP Meteor is about finding a better method to monitor the operation of hardware components, including the hardware code into the regression test process. The fast-changing customer demand lead to a frequent upgrading in Meteor solutions while modifications in existing Meteor architecture may bring unforeseen outcomes to some specific types of printheads. Current regression test procedure for hardware components is actual printing on rig. This is a time-consuming process and usually a cumbersome job when number of target hardware increases. By pseudo printing specific test pattern, collecting and analysing necessary signals from hardware using software, testing procedure will be simplified with potentially higher accuracy, bringing higher working efficiency into company operation.

Apart from the main project about hardware testing as mentioned above, I was also involved in other project and allocated other jobs. Technical projects include developing testboards, which performs quick check of manufacture errors before mass production. On the business side, I was responsible to provide customer support for those from non-English speaking countries, realising the direct communication between the engineers at both sides.

This placement project is closely related to my college course content and requires me to apply and develop my knowledge in practical situations. In the placement, I had the opportunity to broaden my skill set by learning and practicing PCB design, FPGA development and windows application development, and hence, find my interest in some particular engineering work. TTP Meteor is growing at an incredible speed in the past few years. The business strategies this company is following, which explored the new market and contributed to the independency of TTP Meteor is also impressive. This placement not only practiced my technical skills, but also provided me with a broader view about company management and business operation.

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# 2. Company Overview

TTP Group is a world-leading technology and development company, focusing on meeting needs of companies through the use of advanced technology and innovations. It is located in a Science Part near Cambridge. The main business in TTP Group is technical consulting, providing ideas and designing solutions to clients. It has been playing a pioneering role in a broad range of areas including drug discovery, pharmaceutical automation, laboratory instrumentation, digital printing, wireless communications and consumer products.

Twenty-five years ago, the Technology Partnership was established, which quickly expanded and reorganised under the new parent, TTP Group plc. As the business has grown, new companies have been created and flourished. Now TTP Group has more than three hundreds technical consultants and scientists, working in several independent enterprises within the group, such as TTP Labtech, TTP Venture Fund, etc.

TTP Meteor was born with TTP, closely involved in digital printing for decades, and has officially become an independent company this year, specialised in providing industrial-used printhead driver systems. TTP Meteor is not only limited in consulting business, but also including hardware production and customer support into the business. Apart from providing designs and prototyping solutions, Meteor also offers its own software and hardware architecture which is applicable to twenty different print head in market. This strategy contributes to the revenue increase of 80% every year in the past few years and transfer TTP Meteor from a consulting group to an independent company. Now it has fourteen engineers and consultants, and a number of salesmen based in Europe, Asian and America.

//Add introduction to printing industry, difference between industries used printers and commercial-used printers. Why this company survives

Meanwhile, the Meteor hardware and software are optimised differently to achieve the best performance out of different printhead.

I came to TTP Meteor as a member of the research and development team. TTP Meteor organises monthly company business meeting, showing the operation and situation of the company, such as monthly revenue report, customer demand and human resource. In addition, research and development team has weekly meeting, discussing the progress and working plan of individuals as well as the team.

Meteor

Role and responsibility

The company operation developed my understanding in business and management.

Through working closely with customers and participating conference, I also improved my skills in interacting with different customers.

TTP Meteor is now growing in a rapid speed with more than one hundred percent increase in revenue last year. The intensive individual responsibility in this small company makes the job allocation clear. How employees with different responsibility coordinate together and guide the company forward is a fascinating process to experience and witness.

# 3. Project Description

The project I was responsible for during this placement is developing a procedure which inspects and analyses hardware operations, including hardware components into the regression test procedure. Before explaining any details, an overview of the typical design architecture, ‘the Meteor Architecture’, will be helpful in acknowledging the aim and working principles of this project.

## 3.1 Project Background

TTP Meteor has its origin in consulting industry, which is famous for fierce competition and changeable environment. To satisfy the fast-changing demand from customers, Meteor developed its own architecture, providing a highly flexible and adaptive solution for printhead driver systems. By using the Meteor Architecture, users are able to select or switch their printhead options among the twenty supported printheads, with low cost, to maximise their benefit.

**User Input**

**Windows Application**

**Print Controller Card**

**Head Driver Card**

**Head Driver Card**

**… …**

**Print Head**

**Print Head**

**… …**

Windows Application:

User interface and command control

Head Driver Card (HDC):

Driver unit for different printheads

Print Controller Card (PCC):

Central hardware control unit

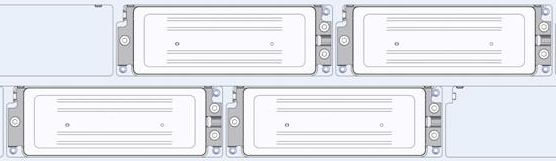
**Figure 1.** The Meteor Hardware Architecture (the blue area).

Figure 1 illustrates the basic Meteor Hardware Architecture, which realised the complete user control over multiple printheads. The Meteor Architecture consists of three major components: software application, print controller card (PCC) and head driver card (HDC).

Software application is the user interface, which provides complete user control over configurations, offering various printing choices for different practical situations. The fast image transmission allows the high printing speed of printhead, which is the basis of high productivity in printing industry.

Print Controller Card (PCC) is the control hub, distributing image data and command to multiple head drivers. It coordinates multiple head drivers to accomplish a more complicated printing job, for instance, printing in seamless and large scale, or printing with a resolution, which is higher than that of the printhead. Figure 2 shows an example of printhead alignment to obtain larger printing scale.

Head Driver Card (HDC) is the hardware designed to achieve the best performance out of print head. Twenty different types of printheads are supported with specialised HDCs, providing a range of choices for customer. Each type of HDC is optimised in different ways depending on printhead choice. For instance, different printheads require different waveform across the piezoelectric material to fire ink drop. Also some ink type desires suitable operation temperature or UV light to obtain the best performance.



**Figure 2.** Multiple printhead alignment strategy to increase printing scale

However, high flexibility and adaptability of this architecture introduces risk in reliability. Fast-changing environment requires Meteor to upgrade or modify our design, both software and hardware, frequently to satisfy customer’s changeable demand. It brings the challenge that the any revision or upgrade performed may or may not support all print head types since they are usually designed for customer with specific printhead preference. Therefore, to ensure the change on part of the architecture does not damage the rest, a regression test procedure is necessary.

Due to the limitation on time, equipment and human resource, it will be cumbersome and impractical to perform actual printing with all supported printheads in the company. This brings in the motivation of my project. By inspecting all necessary signals at hardware output, sufficient information can be collected to distinguish a ‘good’ or ‘bad’ printing behaviour. This test procedure is universal and applicable to all printheads. The Meteor Architecture will be examined on computer so this test does not require actual connection to printhead or ink system, and therefore expected to be simple and convenient. //Need further simplification

## 3.2 Project Design Procedure

This is a relatively large project covering from low-level hardware design to high-level user interface design and it is the main project during the five months. Therefore, an appropriate job organisation and time plan is essential before any technical work begins.

To start with, I worked on obtaining an overview my project. Regression test is a general concept, there are many possible ways to realise it. The real question then becomes how to choose the optimal solution to run in TTP Meteor, considering deliverables, budget and time limit. First of all, I familiarise myself with the company business and operation to develop the understanding about how my project is supposed to fit into this company.

The main function of my project is to perform universal test on a range of printheads, which will mainly be used in two ways in this company. First of all, as is mentioned in previous section, the testing process will be included in regression test procedure, which happens at the end of the development cycle when deadline is approaching. Secondly, our customer support provides service to investigate and repair the faulty boards returned from our customer, which will also help us improving our product. Our big customer usually sends a large number of boards to repair or replacement, which is a time-consuming process. Universal test will help simplify the board review process before sending them back to customers. In both of the situations above, testing procedure is desired to be time-saving and intuitive, which consumes the least amount of time possible to determine whether a test is a success and failure, while detailed information may not be essential.

**Print Head**

**Figure 2.** Universal test on the Meteor Architecture

**User Input**

**The Meteor Architecture**

**Monitor**

**Universal Test**

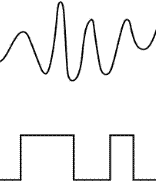
Figure 2 shows how universal test operates with the Meteor Architecture. By comparing the collected output signals of the Meteor Architecture to the expected signals depending on user settings, test will generate the result that whether the printing behaviour is successful.

Following the project overview above, I start to think about the possible approaches of the implementation. The implementation of the test procedure design can be divided into three major questions: How to collect data from various types of printhead in order to keep the testing procedure universal? How to transfer collected data back to computer in a reliable way at a reasonable speed? How to perform reliable analysis and distinguish correct and faulty signals for different signal types? Solutions to these questions constitute the blueprint of my design, which will be discussed in detail in next section.

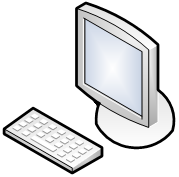
After acknowledging technical work involved in this project, I was then able to outline the time plan throughout this placement, considering detailed jobs involved and contingency events. This will also be provided with more details in the following section. This design process of this project is such an instructive and helpful experience, from which I learnt to understand and organise a project involving multiple stages.

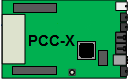
## 3.3 Technical Details

To find the optimal method to implement the universal test procedure, I familiarise myself with the hardware devices and software architecture. After comparing several different possible methods, I decided to use an existing type of PCC, which is an FPGA board with microcontroller and USB connection. This specific type of PCC has the name of ‘PCC-X’, which is specially designed with board-to-board connectors, providing extra possibilities on functionality. This is considered to be the optimal solution due to the low cost and large resource available to work on an existing product. //to simplify



**Signal Inputs**





**USB 2.0**

**Microcontroller**

**FPGA**

**Figure 3.** Details of hardware components for universal test

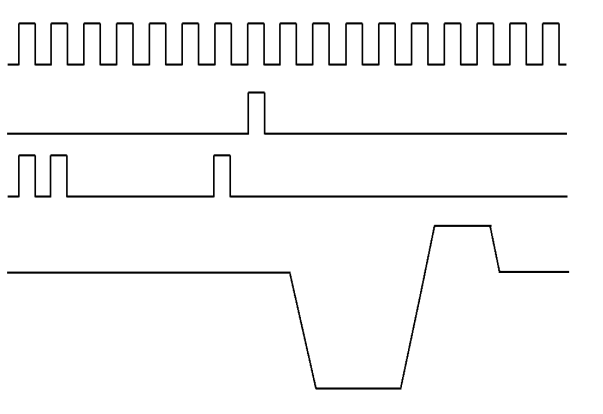
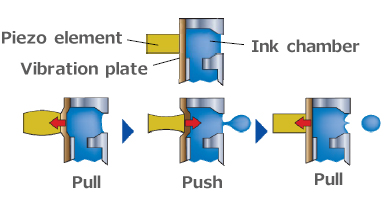
Figure 3 illustrates the structure of regression test design, using an adaptor to access the output of various HDC types and sending data to PC through FPGA, microcontroller and USB. Due to the limitation on number of pins available on FPGA, it is impractical to monitor all HDC outputs simultaneously. Instead, FPGA uses adaptor to scan through signal channels sequentially, monitor the each signal channel for one printing cycle only.

Technical skills and knowledge desired include PCB schematic and layout design, FPGA development using VHDL and .net user interface design using C#. Design details are explained in the following sections.

## 3.3.1 Adaptor board design

Understanding the signal outputs of the Meteor Architecture and the working principle of printhead is essential before processing them. In Meteor Architecture, HDC is at the bottom of the hierarchy, which connects printhead directly. So the outputs of HDC are what we need to focus on.

Figure 4 shows what input signals to printhead are like. Serial data are clocked into printhead by latch signal, followed by an analogue waveform which drives the piezo crystal to fire ink drop. More details about piezoelectronic inkjet print are included in Figure 5.



**CLK**

**Latch**

**Data**

**Waveform**

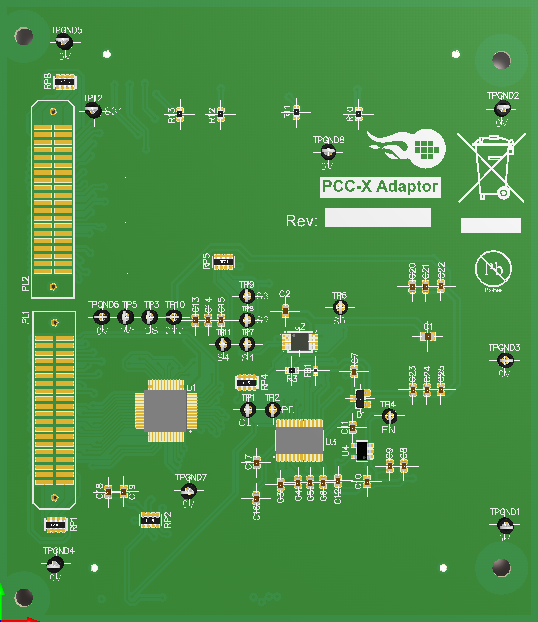
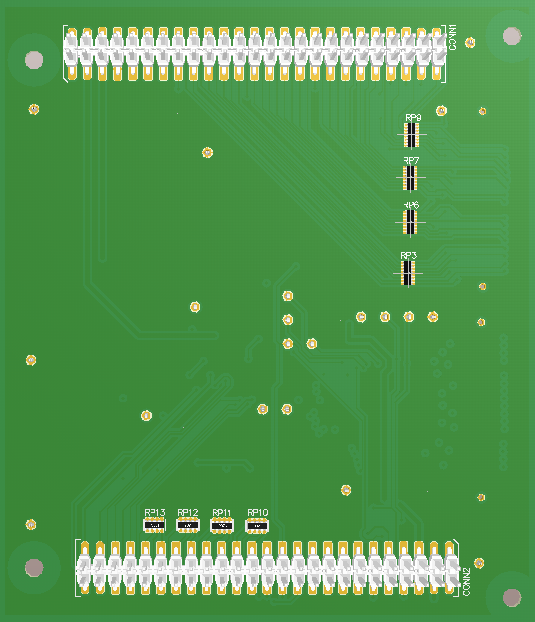
**Figure 4.** Data sequencing diagram

**Figure 4.** Driving signals for printhead

**Figure 5.** Piezo technology to jet ink drop

Piezoelectric inkjet is based on the phenomenon of piezoelectricity where the physical shape of piezoelectric material bends and vibrates with the voltage applied to them. When the voltage is reversed, material bends to the opposite size rapidly, firing ink drop at a high speed. With careful design of waveform, ink drop size can be controlled in micrometre, allowing high printing resolution and precision.

In my project, latch signal is used to separate printing cycles. There are 32 analogue channels and 32 digital channels available, providing sufficient capacity to monitor a range of HDCs. Signals are sampled at 20 Msps to avoid aliasing. Analogue waveforms are passed through a noise-removal filter to analogue-to-digital converter before being collected by FPGA.



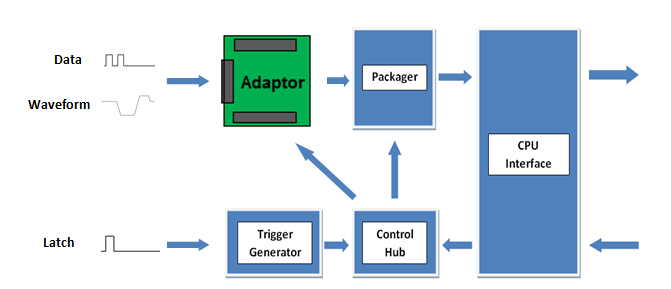
**Figure 6.**3D layout model of PCC-X Adaptor

Figure 6 shows the 3D mode l of the adaptor board. Although the functionality of the adaptor board is not complicated, making this board reliable and safe does require extra techniques. Many circuit protection methods are applied to minimise the risk when high-voltage faulty signal are present. Protection diodes and resistors are placed to avoid damaging FPGA by maintaining external signals at a reasonable level. Ground wires are inserted between high frequency signals to minimise the crosstalk. Path of the clock signal is designed not to cross any other signal to minimise the effect of noise. Control signals of the multiplexer and the Analogue-Digital Converter are designed to have similar length to minimise skew.

Compared to complexity of other PCB design in this company, the Adaptor board I designed is trivial. However, it turns out to be the most cumbersome part in this project, due to manufacture standards and conventions I have to follow to make the board meet the requirements to be produced. The requirements are specific and cover all the details such as hole-to-hole clearance, minimum annular ring size, polygon clearance, etc. Engineers in this company sometimes need to adjust these standards based on their experience to reduce the risk of manufacture failure.

## 3.3.2 FPGA design

FPGA acts as an intermediary between software layer and hardware layer. It reads the commands from software, controls the operation of adaptor board, collects and delivers data packets back to software. How to execute the universal test is defined in this part.



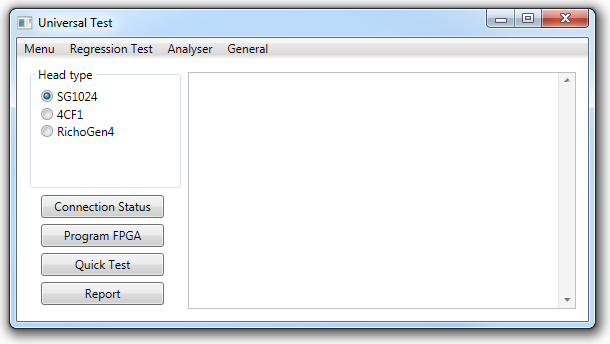
**Digital Data**

**Figure 7.** Intuitive block diagram of my FPGA design

Figure 7 illustrates the intuitive operation mechanism of FPGA blocks with the adaptor board. Latch signal is used to trigger the test. Samples taken from each channel are labelled, packaged then send through microcontroller interface to PC. During the FGPA development, I found the content learned in college VHDL course and digital electronics particularly useful. The long progression delay between FPGA and microcontroller interface makes the command signals difficult to meet timing requirement at system clock frequency. It is eventually fixed by moving the FPGA output blocks to a slower time domain and introducing pipelining.

Implementing the FPGA components is a practical and demanding job. As the designer, I not only need to determine the details about the testing steps and packaging methods, but also desire to assemble the individual blocks and functionalities together into a compact system. The work involved in debugging the interfaces is usually multiples of the work of implementing individual functionalities.

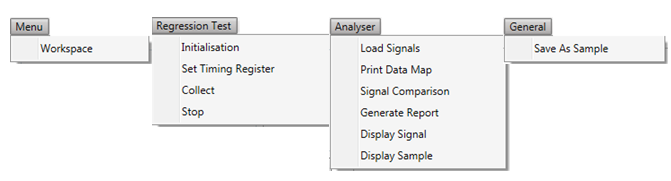
## 3.3.3 User Interface Development

A WPF application based on .Net framework has been developed to monitor the universal testing process, aiming to provide reliable and informative data analysis while minimise the complexity of the testing process. Figure 8 shows the main interface with the intuitions of test procedure and function categories.

**Figure 8.** Main window of universal test application

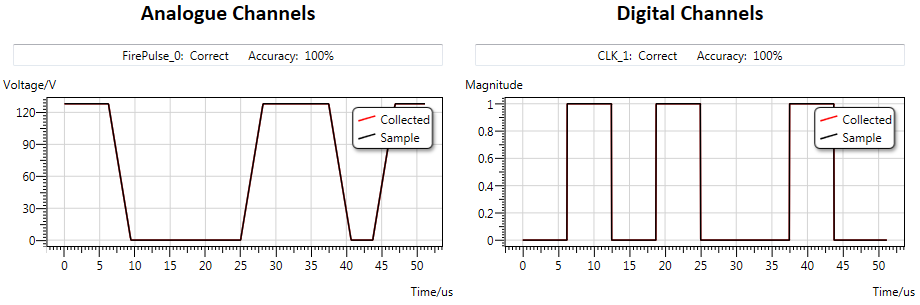
The user interface design involves three main functional areas: data entry, sequence control and data display.

First of all, the application customises the test process by accessing user configurations such as printhead type, print rate, and signal declarations. Parameter settings and user input are saved in command registers on FPGA. Labelled samples are sent through microcontroller fast data bus running at 80Msps, raw data in byte code are converted into readable format for further analysis in software.

Secondly, the application covers the entire testing process, where the individual steps are highly dependent on each other. User might obtain corrupted data or overload CPU by creating too many threads if unexpected operations are performed. Accordingly, a series of conditional variables are used to indicate the state of test process, which maintain the procedure under control and reduces the risks of introducing bug by user operation. Error messages are provided to guide user to follow the correct test steps.

**Figure 9.** Drop-down menu bars

Also, by providing detailed and low-level functions under drop-down menus such as FPGA command register control, shows as Figure 9, this application provides developers with sufficient freedom over the testing process. In the other side, individual functions are combined into a ‘Quick Test’ function, which minimise the user input required for convenience.



**Figure 9.** Graphic display of data in analogue and digital channels

Thirdly, an external library named ‘Dynamic Data Display’ is used to provide user-friendly interface to present data, since C# is not particularly dedicated in graphics. Currently two types of comparing methods are implemented, providing direct comparison or calculating the cross correlation between collected data and pre-saved sample data. Any obvious deviation from the sample data can be observed from the graph, while the accuracy estimates the similarity of signals, which is useful if noise or time offset exist in collected data, resulting in unnoticeable and insignificant differences.

//More work

Considering the nature of the two types of signals, waveform is an analogue signal which may still be considered correct if it is not identical for all printing cycles. As long as the waveform reached desired voltage and correct time, it drives nozzles in a proper way and is considered to be ‘Good’. While digital signals have 1s and 0s only, if exceptional value is obtained or the faulty values appear at the wrong time interval, this signal can be categorized as ‘Bad’. Digital signals which are sampled at high system frequency are then downsampled to the serial data clock for printhead. Downsampling reduce the effect of noise and time shift in digital signals. It is a reasonable method to justify digital signal from the perspective of how printhead receive them.//More potential improvement

User interface design is a time-consuming but entertaining process. Starting from implementing basic functions to interface with hardware, to finalise analysis and present graphic results to user, the application have to accomplish a large amount of work in the background which is hidden from user and only present the most concise content to user. Implementing bug-free functions is the most basics in this application. Based on that, there are many different ways to combine primitive functions to high-level functions. Abstracting and presenting functionalities to user requires clear and logical sense of sequence control, which should guide user through the testing procedure. Another point which some programmer might downplay is user experience. In my application, many function such as programming FPGA and data collection do not finishes instantly. Separate threads are created to prevent application from stall. Efficiency is also improved by running different analysis parallel to each other.

## 3.3.4 Project Planning

After investigating possible approaches to implement the testing system and estimating the types and amount of work involved, a detailed project plan is drafted to manage time and instruct design procedure. Please see Figure 10.

**Figure 10.** Project timeline plan

When outlining this time plan, sufficient time is added at the end of each designing stage, marked by different colours of tasks. Despite the consideration of contingency, the actual development process did not follow the plan. I finished FPGA and software application earlier than the planned date, while the PCB design was paused and postponed for two months. This is caused by a customer order of our new product, which will due in October. Before the mass production of the new product, a batch of manufactured sample will be sent to us to check manufacture error in advance. Therefore, I paused my project and start working on designing testboards, which examine

## 3.3.5

# 4. Project Refection

Challenge,

Personal and Professional lessons

Future work

Relevance to degree course

Thinking and Planning of future career

# 5. Conclusion